



HE83148 APPROVAL AND TOOLING FORM

COMPANY NAME: _____ DATE: _____
 PART NUMBER: HE83148
 PROJECT NAME: _____
 CODE NUMBER: HE83148-
 PRODUCTION NUMBER _____ (by King Billion)

PRODUCTION INFORMATION:

Package Type:	Package Form (_____)	Chip Form
Ink:	Line one – _____ Line two – _____ Line three – _____	
Remark:	_____	

CODE INFORMATIN:

File Name: _____
Check Sum: _____
Object Code length: _____

DEVICE OPTION:

Operation Voltage: Two-Battery Other(_____)

Mask Options:

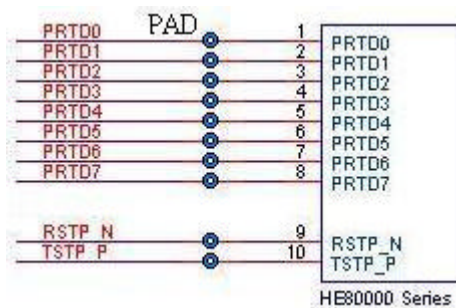
NAME	DESCRIPTION	Mask Option	
MO_PORE	Internal Power On Reset	Disable(0)	Enable(1)
MO_FCK MO_SCKN	Clock Mode Select	Dual Clock (10) Fast Only (11)	Slow Only (00)
MO_FXTAL	Osc. Type of Fast Clock	RC(0)	X' tal(1)
MO_SXTAL	Osc. Type of Slow Clock	RC(0)	X' tal(1)
MO_WDTE	Watch Dog Timer	Disable(0)	Enable(1)
MO_FOSCE	Fast Clock Source Select	Internal(0)	External(1)
MO_FRCL_S[2:0]	Internal Fast Clock Rate Select (If internal clock is selected.)	~=990KHz(000) ~=1.3MHz(010) ~=2MHz(100) ~=3.9MHz(110)	~=1.1MHz(001) ~=1.6MHz(011) ~=2.6MHz(101) ~=6.5MHz(111)
MO_LCDBS[2:0]	LCD Bias Resistor	000: 30K 010: 90K	001: 60K 011: 120K



		100: 210K	101: 240K
		110: 270K	111: 300K
MO_DPP[0]	Port D Bit 0 Configuration	Open-drain	Push-pull
MO_DPP[1]	Port D Bit 1 Configuration	Open-drain	Push-pull
MO_DPP[2]	Port D Bit 2 Configuration	Open-drain	Push-pull
MO_DPP[3]	Port D Bit 3 Configuration	Open-drain	Push-pull
MO_DPP[4]	Port D Bit 4 Configuration	Open-drain	Push-pull
MO_DPP[5]	Port D Bit 5 Configuration	Open-drain	Push-pull
MO_DPP[6]	Port D Bit 6 Configuration	Open-drain	Push-pull
MO_DPP[7]	Port D Bit 7 Configuration	Open-drain	Push-pull
MO_14PP[0]	Port 14 Bit 0 Configuration	Open-drain	Push-pull
MO_14PP[1]	Port 14 Bit 1 Configuration	Open-drain	Push-pull
MO_14PP[2]	Port 14 Bit 2 Configuration	Open-drain	Push-pull
MO_14PP[3]	Port 14 Bit 3 Configuration	Open-drain	Push-pull
MO_14PP[4]	Port 14 Bit 4 Configuration	Open-drain	Push-pull
MO_14PP[5]	Port 14 Bit 5 Configuration	Open-drain	Push-pull
MO_14PP[6]	Port 14 Bit 6 Configuration	Open-drain	Push-pull
MO_14PP[7]	Port 14 Bit 7 Configuration	Open-drain	Push-pull
MO_LIO14[0]	Port 14 Bit 0 I/O or LCD bit	I/O	LCD
MO_LIO14[1]	Port 14 Bit 1 I/O or LCD bit	I/O	LCD
MO_LIO14[2]	Port 14 Bit 2 I/O or LCD bit	I/O	LCD
MO_LIO14[3]	Port 14 Bit 3 I/O or LCD bit	I/O	LCD
MO_LIO14[4]	Port 14 Bit 4 I/O or LCD bit	I/O	LCD
MO_LIO14[5]	Port 14 Bit 5 I/O or LCD bit	I/O	LCD
MO_LIO14[6]	Port 14 Bit 6 I/O or LCD bit	I/O	LCD
MO_LIO14[7]	Port 14 Bit 7 I/O or LCD bit	I/O	LCD
MO_15PP[0]	Port 15 Bit 0 Configuration	Open-drain	Push-pull
MO_15PP[1]	Port 15 Bit 1 Configuration	Open-drain	Push-pull
MO_15PP[2]	Port 15 Bit 2 Configuration	Open-drain	Push-pull
MO_15PP[3]	Port 15 Bit 3 Configuration	Open-drain	Push-pull
MO_15PP[4]	Port 15 Bit 4 Configuration	Open-drain	Push-pull
MO_15PP[5]	Port 15 Bit 5 Configuration	Open-drain	Push-pull
MO_15PP[6]	Port 15 Bit 6 Configuration	Open-drain	Push-pull
MO_15PP[7]	Port 15 Bit 7 Configuration	Open-drain	Push-pull
MO_LIO15[0]	Port 15 Bit 0 I/O or LCD bit	I/O	LCD
MO_LIO15[1]	Port 15 Bit 1 I/O or LCD bit	I/O	LCD
MO_LIO15[2]	Port 15 Bit 2 I/O or LCD bit	I/O	LCD
MO_LIO15[3]	Port 15 Bit 3 I/O or LCD bit	I/O	LCD
MO_LIO15[4]	Port 15 Bit 4 I/O or LCD bit	I/O	LCD
MO_LIO15[5]	Port 15 Bit 5 I/O or LCD bit	I/O	LCD
MO_LIO15[6]	Port 15 Bit 6 I/O or LCD bit	I/O	LCD
MO_LIO15[7]	Port 15 Bit 7 I/O or LCD bit	I/O	LCD

NOTE :

1. For accessing any address large than 64KB, users must update TPP first, TPH then TPL. Only by this order, the pre-charge circuit of ROM will work correctly. 5us waiting is necessary before LDV instruction is executed since Data ROM is a low speed ROM. Users can not emulate this accessing process in ICE. So 5us delay should be added by firmware.
2. LCD driving circuit must be turn off before IC goes into sleep mode.
3. Please bonds the TSTP_P, RSTP_N and PRTD[7:0] with test point on PCB (can be soldered and probed) as you can, then KB can do some IC testing job on PCB. Neither VDD nor GND connection is necessary for TSTP_P. The following figure is an example (Testing point with through hole).



4. LV3 must small than 9.0 Volt. Otherwise IC may breakdown.

DEVICE USAGE CHECK: (for double check purpose only)

Clock Mode:	Dual	Fast	Slow	Idle	Sleep
Reset Usage:	External		Internal		
Watch Dog Timer Usage:	WDT				
I/O Usage:	_____ Input,		_____ Output,		_____ Bi-directional
RAM Usage:	Total _____ Byte is used.				
ROM Usage:	Total _____ KB is used, _____ KB is utilized as program ROM.				
Timer Usage:	Timer I		Timer II		Time-base
LCD Usage:	_____ COM,		_____ SEG		
Speech Usage:	PWM Output		D/A Output		
OPAMP Usage:	As comparator		As OPAMP		

APPROVED BY: ICE ROMLESS DEMOBOARD OTHER(_____)

COMMENTS :

<p>CUSTOMER APPROVAL BY:</p> <p>SIGNATURE: _____</p> <p>PRINTED NAME: _____</p> <p>TITLE: _____</p>	<p>K.B. CONFIRMATION BY:</p> <p>SIGNATURE: _____</p> <p>PRINTED NAME: _____</p> <p>TITLE: _____</p>
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