



HE83R126 APPROVAL AND TOOLING FORM

COMPANY NAME: _____ DATE: _____
 PART NUMBER: HE83R126
 PROJECT NAME: _____
 CODE NUMBER: HE83R126-
 PRODUCTION NUMBER _____ (by King Billion)

PRODUCTION INFORMATION:

Package Type:	Package Form (_____)	Chip Form
Ink:	Line one – _____	
	Line two – _____	
	Line three – _____	
Remark:	_____	

CODE INFORMATIN:

File Name: _____
Check Sum: _____
File Size: _____

DEVICE OPTION:

Operation Voltage: Two-Battery Three-Battery Other(_____)

Mask Options:

NAME	DESCRIPTION	Mask Option
MO_PORE	Internal Power On Reset	Disable(0) Enable(1)
MO_FCK MO_SCKN	Clock Mode Select	Dual Clock (10) Fast Only (11) Slow Only (00)
MO_FXTAL	Osc. Type of Fast Clock	RC(0) X' tal(1)
MO_SXTAL	Osc. Type of Slow Clock	RC(0) X' tal(1)
MO_WDTE	Watch Dog Timer	Disable(0) Enable(1)
MO_FOSCE	Fast Clock Source Select	Internal(0) External(1)



MO_FRCL_S[2.0]	Internal Fast Clock Rate Select (If internal clock is selected.)	~=990KHz(000) ~=1.1MHz(001) ~=1.3MHz(010) ~=1.6MHz(011) ~=2MHz(100) ~=2.6MHz(101) ~=3.9MHz(110) ~=6.5MHz(111)
MO_LVRG	LCD REGULATOR	Disable(0) Enable(1)
MO_DPP[0]	Port D Bit 0 Configuration	Open-drain Push-pull
MO_DPP[1]	Port D Bit 1 Configuration	Open-drain Push-pull
MO_DPP[2]	Port D Bit 2 Configuration	Open-drain Push-pull
MO_DPP[3]	Port D Bit 3 Configuration	Open-drain Push-pull
MO_DPP[4]	Port D Bit 4 Configuration	Open-drain Push-pull
MO_DPP[5]	Port D Bit 5 Configuration	Open-drain Push-pull
MO_DPP[6]	Port D Bit 6 Configuration	Open-drain Push-pull
MO_DPP[7]	Port D Bit 7 Configuration	Open-drain Push-pull
MO_15PP[0]	Port 15 Bit 0 Configuration	Open-drain Push-pull
MO_15PP[1]	Port 15 Bit 1 Configuration	Open-drain Push-pull
MO_15PP[2]	Port 15 Bit 2 Configuration	Open-drain Push-pull
MO_15PP[3]	Port 15 Bit 3 Configuration	Open-drain Push-pull
MO_15PP[4]	Port 15 Bit 4 Configuration	Open-drain Push-pull
MO_15PP[5]	Port 15 Bit 5 Configuration	Open-drain Push-pull
MO_15PP[6]	Port 15 Bit 6 Configuration	Open-drain Push-pull
MO_15PP[7]	Port 15 Bit 7 Configuration	Open-drain Push-pull
MO_LIO15[0]	Port 15 Bit 0 I/O or LCD bit	I/O(0) LCD(1)
MO_LIO15[1]	Port 15 Bit 1 I/O or LCD bit	I/O(0) LCD(1)
MO_LIO15[2]	Port 15 Bit 2 I/O or LCD bit	I/O(0) LCD(1)
MO_LIO15[3]	Port 15 Bit 3 I/O or LCD bit	I/O(0) LCD(1)
MO_LIO15[4]	Port 15 Bit 4 I/O or LCD bit	I/O(0) LCD(1)
MO_LIO15[5]	Port 15 Bit 5 I/O or LCD bit	I/O(0) LCD(1)
MO_LIO15[6]	Port 15 Bit 6 I/O or LCD bit	I/O(0) LCD(1)
MO_LIO15[7]	Port 15 Bit 7 I/O or LCD bit	I/O(0) LCD(1)

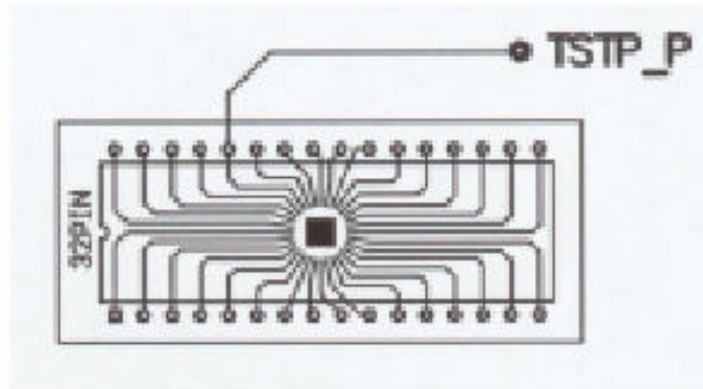
NOTE:

LCD driving circuit must be turn off before IC goes into sleep mode.

Please bonds the TSTP_P with test point on PCB (can be soldered and probed) as you can, then KB can do some IC testing job on PCB.

Neither VDD nor GND connection is necessary for TSTP_P.

The following figure is an example (Testing point with through hole).



DEVICE USAGE CHECK: (for double check purpose only)

Clock Mode:	Dual	Fast	Slow	Idle	Sleep
Reset Usage:	External		Internal		
Watch Dog Timer Usage:	WDT				
I/O Usage:	_____Input,		_____Output,		_____Bi-directional
RAM Usage:	Total_____Byte is used.				
ROM Usage:	Total_____KB is used,_____KB is utilized as program ROM.				
Timer Usage:	Timer I		Timer II		Time-base
LCD Usage:	_____COM,		_____SEG		
Speech Usage:	PWM Output			D/A Output	
OPAMP Usage :	As comparator			As OPAMP	

APPROVED BY: ICE ROMLESS DEMOBOARD OTHER(_____)

COMMENT:

<p>CUSTOMER APPROVAL BY:</p> <p>SIGNATURE: _____</p> <p>PRINTED NAME: _____</p> <p>TITLE: _____</p>		<p>K.B. CONFIRMATION BY:</p> <p>SIGNATURE: _____</p> <p>PRINTED NAME: _____</p> <p>TITLE: _____</p>
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